REMARKS

Claims 1-28 are pending, of which claims 1, 9, 17, and 21 are in independent form.

Claims 3, 11, and 23 have been amended by way of the present response solely to address certain informalities.

No new matter is introduced.

Favorable reconsideration of the present application as currently constituted is respectfully requested.

Regarding the Claim Objections

Claims 3, 11, and 23 stand objected to because of certain informalities. Applicant has appropriately amended claims 3, 11, and 23 responsive to the Examiner's comments in this regard. It is therefore believed that these claim objections have been overcome or otherwise rendered moot by the present response.

Regarding the Allowable Subject Matter

Applicant gratefully appreciates the indication in the current Office Action that claims 3-8, 11-16, and 23-28 "are objected to as being dependent upon a rejected base claim, but would be rewritten in independent form including all of the limitations of the base claim and any intervening claims". In view of the arguments set

forth below, it is believed that these claim objections have been overcome and that claims 3-8, 11-16, and 23-28 are allowable in their present form.

Regarding the Claim Rejections

In the pending Office Action, claims 1, 2, 9, 10, 17-20, 21, and 22 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,128,971 to Schmitz (the *Schmitz* reference). In connection with these §102(b) rejections, the Examiner has commented as follows with respect to base claim 1:

> (1) A method for providing interface compatibility between two hierarchical collections (*"a different design library or...another portion of the same library"- Application, paragraph 15)* of integrated circuit (IC) design objects, comprising (col.53,ll.45-55):
>
> establishing an associative correspondence between a design object from a first hierarchical (assignment dependencies/fanout) collection and a design object from a second hierarchical collection (The product term resources in a programmable logic block may be thought of as the abilities of the males in the marriage problem. The logic equations (females) are "compatible" to the degree the macrocells have adequate product term resources present - col.54, ll.14-18) (col.54, ll.5-26; col.59, ll.11-29);
>
> generating a port compatibility map based on determination that a particular associative correspondence includes a pair of design objects, one from each hierarchical collection, that are port-compatible (an initial mapping of the logic equations to the programmable logic block resources is created from the reduced matrix (FIG.42D)- col.55, ll.10-11) (col.54, ll.54-68; col.55,ll.1-20); and

> reducing said port compatibility map to determine a set of design object pairs that allow replaceability between said first and second hierarchical collections (briefly stated the assignment process systematically determines an optimal association between the two populations. In this case, an optimal assignment is a minimum sum of the compatibility measure across all pairs consisting of one member from each population- col.53, II.59-64; the next step in the Hungarian assignment process is to find the minimum uncovered number M and use that number in a second reduction of the matrix...In the second reduction, number M is first subtracted from all uncovered rows, i.e., rows B, C and E and then the number M is added to all covered columns i.e., columns W and Y- col.55, ll.58-65) (col.53, ll.56-66; col.55, ll.38-68; col.56, ll.1-3);

Substantially similar rationale was also applied in the pending Office Action with respect to the rejection of the remaining base claims, i.e., claims 9, 17, and 21.

Applicant respectfully traverses the pending §102(b) rejections and offers the following arguments as support. Base claim 1 is directed to an embodiment for providing compatibility between two hierarchical collections of integrated circuit (IC) design objects. As currently constituted, the embodiment of claim 1 involves, *inter alia*, generating a port compatibility map based on determination that a particular associative correspondence includes a pair of design objects, one from each hierarchical collection, that are port-compatible. Additionally, the port compatibility map is reduced to determine a set of design object

pairs that allow replaceability between the first and second hierarchical collections. Substantially identical features are also recited in the remaining base claims, i.e., claims 9, 17, and 21.

The *Schmitz* reference is directed to a scheme for optimal allocation of resources (i.e., product terms) in a programmable logic device (PLD). In particular, the *Schmitz* scheme employs well known Hungarian assignment process, upon certain simplifying assumptions, to achieve optimal allocation of a number of product terms to a number of logic equations supported by a PLD. See column 53, line 45 to column 54, line 13. In drawing an analogy between the Hungarian assignment process and the problem of resource assignment within a block of a PLD, the product term resources are deemed to be the abilities of the males in the marriage problem with which the Hungarian assignment process was originally concerned. Likewise, the logic equations of a programmable logic block are thought of as the females of the marriage problem. Column 54, lines 14-26. A pair-wise cost matrix is developed and thereafter minimized in order to determine optimal assignment between "males" and "females". Column 54, lines 27-53.

By way of example, FIG. 42A of *Schmitz* describes a scenario of allocating available product term resources A through E (in rows)

to five logic equations, V through Z (in columns), as shown in a 5 x 5 matrix. The rows are referred to as slots where a particular logic equation can be placed. The value at the intersection of a row and a column is the cost associated with using the row's product term for that particular logic equation identified in the column. Column 54, lines 54-65. A reduced matrix is generated after certain row and column operations, as shown in FIG. 42D, which is further reduced to another matrix as shown in FIG. 42H to find what is referred to as a complete maximal cover. Column 55, line 38 to column 56, line 22.

With regard to applying the foregoing analogy in view of the claimed embodiments of the present patent application, Applicant respectfully submits that it is a mischaracterization to equate the initial matrix of FIG. 42A or the reduced matrix of FIG. 42D to the claimed port compatibility map because these matrices do not disclose or even allude to whether a particular resource (i.e., A through E) is port-compatible with any other resource, or if a particular logic equation (i.e., V through Z) is port-compatible with any other logic equation, or if a particular resource is port-compatible with a particular logic equation in a pair-wise fashion. Essentially, to the extent that the present Office Action appears to draw an equivalence between the logic equations (V through Z)

and the claimed design objects of one hierarchical collection and another equivalence between the product term resources (A through E) and the claimed design objects of another hierarchical collection, there is absolutely no teaching or suggestion of replacing one "design object" with another "design object" in the *Schmitz* reference. Further, reduction of the matrix of FIG. 42D to the matrix of FIG. 42H does not determine a set of design objects that allow replaceability as claimed. Put differently, *Schmitz* is necessarily silent as to the determination of whether a particular resource can be replaced with a particular logic function because the Hungarian assignment process is not at all concerned with the issue of determining entity pairs that allow replaceability between two collections, hierarchical or otherwise.

Based on at least the foregoing reasons, Applicant submits that the pending base claims 1, 9, 17, and 21 are allowable over the applied art of record. Further, dependent claims 2-8 (depending from base claim 1), dependent claims 10-16 (depending from base claim 9), dependent claims 18-20 (depending from base claim 17), and dependent claims 22-28 (depending from base claim 21) are believed to be in condition for allowance in their current form for the same reasons.

PATENT APPLICATION
DOCKET NO.: 200208842-1

SUMMARY AND CONCLUSION

In view of the fact that none of the art of the record, whether considered alone or in combination discloses, anticipates or suggests the pending claims, and in further view of the above remarks and amendments, reconsideration of the Action and allowance of the present patent application are respectfully requested and are believed to be appropriate.

Respectfully submitted,

Dated: 7/3/06

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